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A Comparative Analysis of Various Methods for CMOS Based Integrator Design

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ABSTRACT: Integrator is an important element in various analog and mixed signal circuits like slop based ADC, low pass filters, analog computers, signal processing circuits etc. In this paper we have analysed various methods of designing CMOS based integrator. Finally we compare the various methods like differential op-amp based integrator design, current mode integrator design and linear transconductance based integrator design in terms of power and performance. All the simulations are done in LTSpice.

KEYWORDS:CMOS based Integrator, Differential op-amp, Current Mode Integrator, Linear Transconductance.

I. INTRODUCTION

An Integrator is acomponent which does the mathematical operation of integration on input signal and gives the output signal proportionally. An integrator is a low pass filter whose cut off frequency depends on system parameters like the values of resistor and feedback capacitor. The basicactive integrator circuit is constructed by placing a capacitor C, in the feedback loop of an inverting amplifier as shown in fig.1.

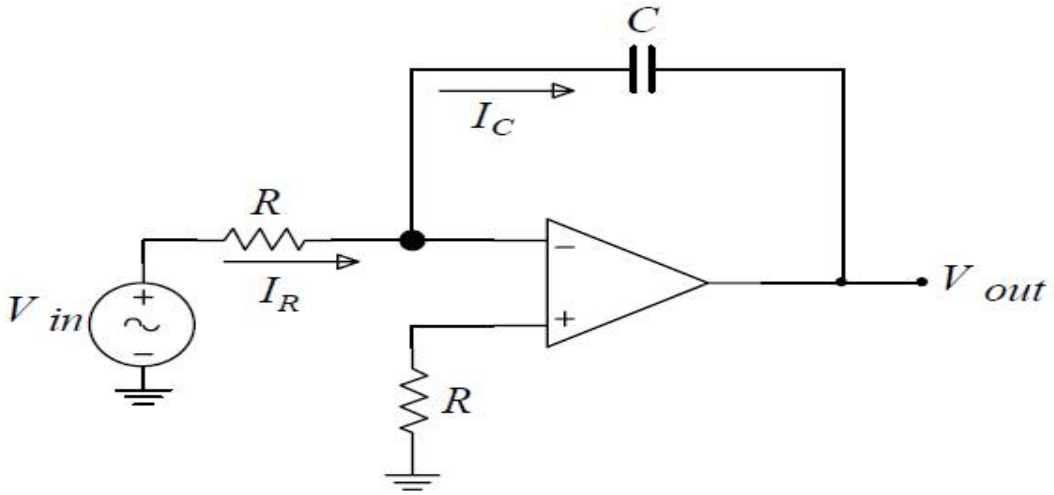

Fig.1. Basic Integrator Circuit

The equation of $V_{out}$is given as

$$Vout(t) = -\frac{1}{RC}\int vin(\tau)\, d\tau + Vout(0) \quad (1)$$

The frequency domain analysis is obtained by expressing the impedance of the feedback components in the complex plane. The transfer function may thus be written as

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$$\frac{Vout}{Vin} = \frac{-Z_C}{Z_R} = \frac{-\frac{1}{j\omega C}}{R} = \frac{j}{\omega RC} \quad (2)$$

The above expression indicates that there is a phase shift of 90°between the input and the output signals. This 90° phase shift occurs at entire band of frequency. Fig.2. shows the logarithmic plot of $\left|\frac{V_{out}}{V_{in}}\right|$ versus frequency

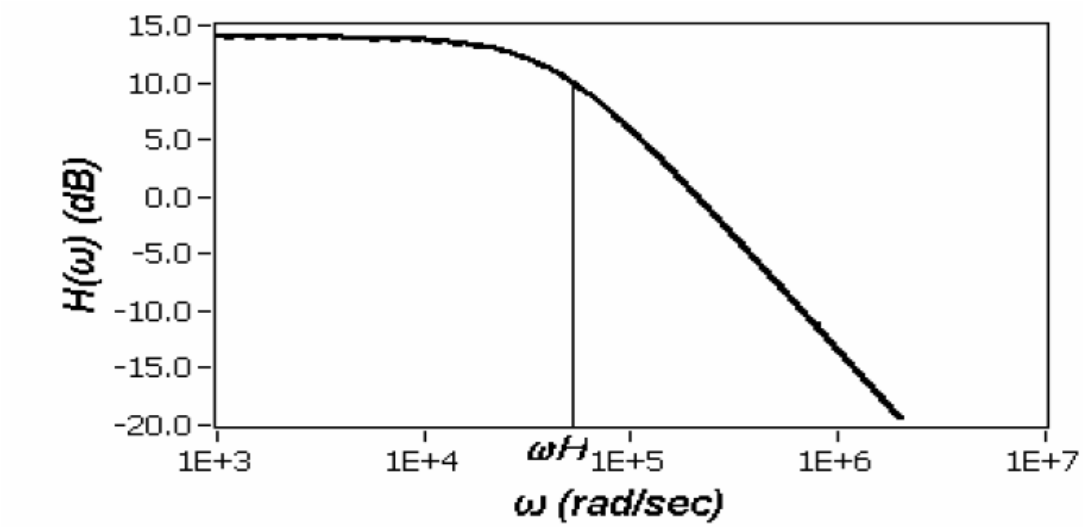

Fig.2. Bode plot of active low pass filter with a gain of 5

II. VARIOUS METHODS OF CMOS BASED INTEGRATOR DESIGN

There are various methods of designing CMOS based integrator like *Two stage Differential Op-amp based Integrator*, *Current Mode Integrator* and *Linear Transconductance based Integrator*. In two stage differential op-amp based approach, the input differential pair provides a large CMRR. Ideally, an op-amp has infinite differential voltage gain, infinite input resistance and zero output resistance. The large output impedance of current mode approach is useful in low voltage and low power applications. While in linear transconductance based approach due to parallel connection of two MOS transistors we can obtain linear V-I characteristics with improved bandwidth and noise performance.

A. Integrator Design with Two Stage Differential Op-amp

Fig.3. shows the circuit configuration of an unbuffered two stage operational amplifier [1]. Table I. shows some custom design specification of op-amp. In the first stage of the operational amplifier transistors (M1, M2, M4 and M5) form - the differential amplifier. The differential amplifier configuration is designed as differential to single ended transformation. The conversion from differential to single ended in this stage, is done by using a current mirror (M1 and M2**).** The current from M4transistor *is* mirrored by M1and M2transistors and subtracted from the current from the transistor M5. The differential current from M4 and M5 is multiplied by the output resistance of the differential input stage gives the single-ended output voltage. This establishes the input of the 2nd gain stage. The 2nd stage is a current sink load inverter. M3is the driver's whereas M8acts as the load. The capacitor Cc is used to reduce the gain at high frequencies and provides the compensation for the operational amplifier. The 1st stage and the 2nd stage circuits use the same reference current; therefore, the bias currents in the two stages will be controlled together.

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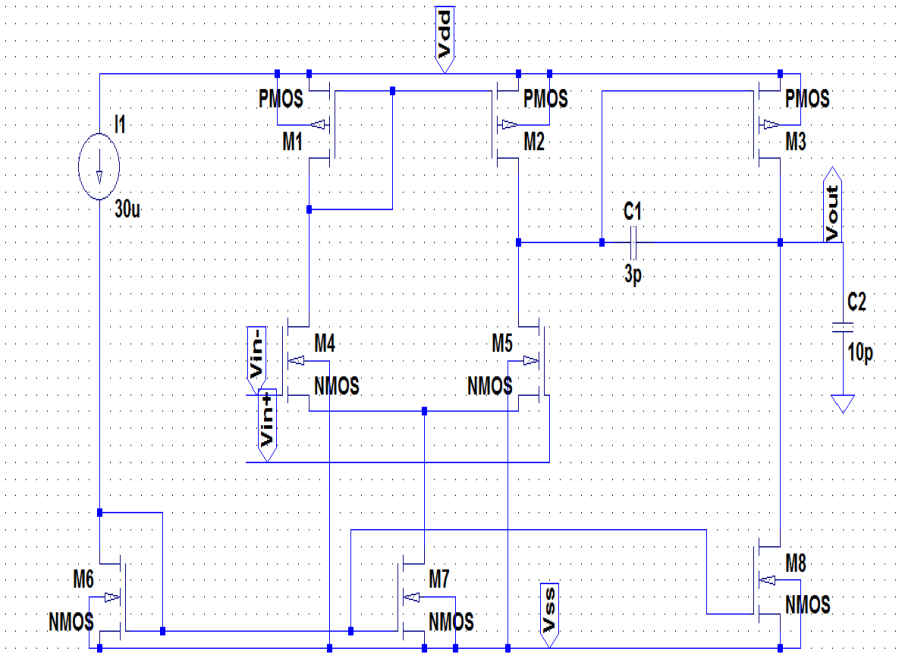

Fig.3. CMOS based differential op-amp[1]

TABLE I.
OPERATIONAL AMPLIFIERS CUSTOM DESIGN SPECIFICATIONS

Specification Names	**Values**
Supply V_{DD}	2.5V
Gain	>70 dB
Slew Rate	10 V/µ sec
Input Common Mode Range	-1 to 2 V
Power Dissipation	<2mW
V_{out}Range	-2V to +2V
C_L	10pF

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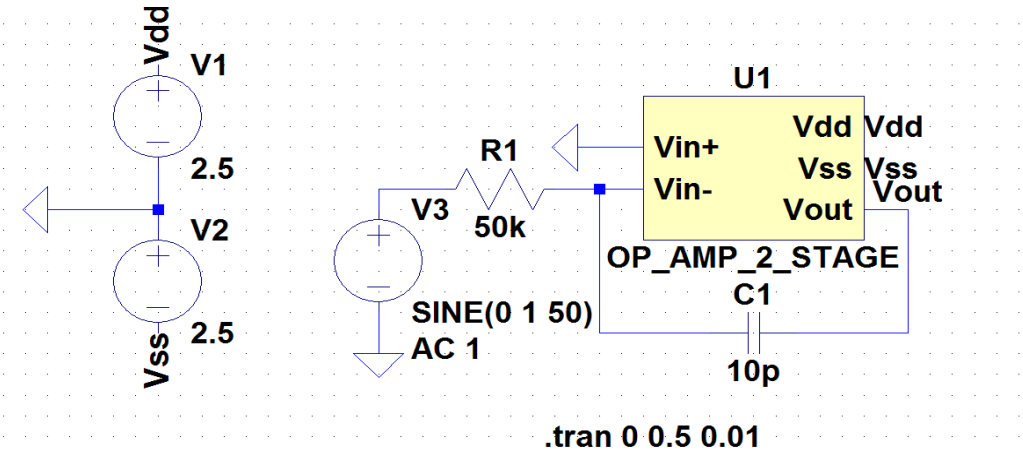

Fig.4. Formation of sub-circuit in LTSpice and Simulation setup

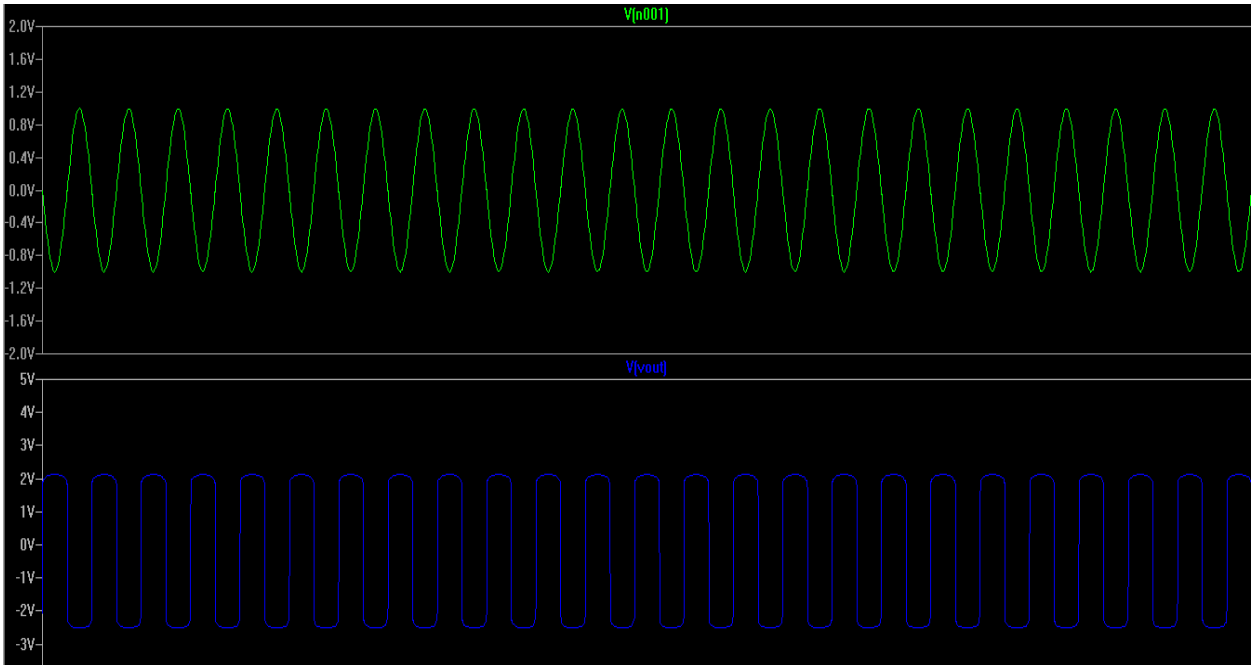

Fig.5. Transient Analysis of Integrator(op-amp_two stage base)

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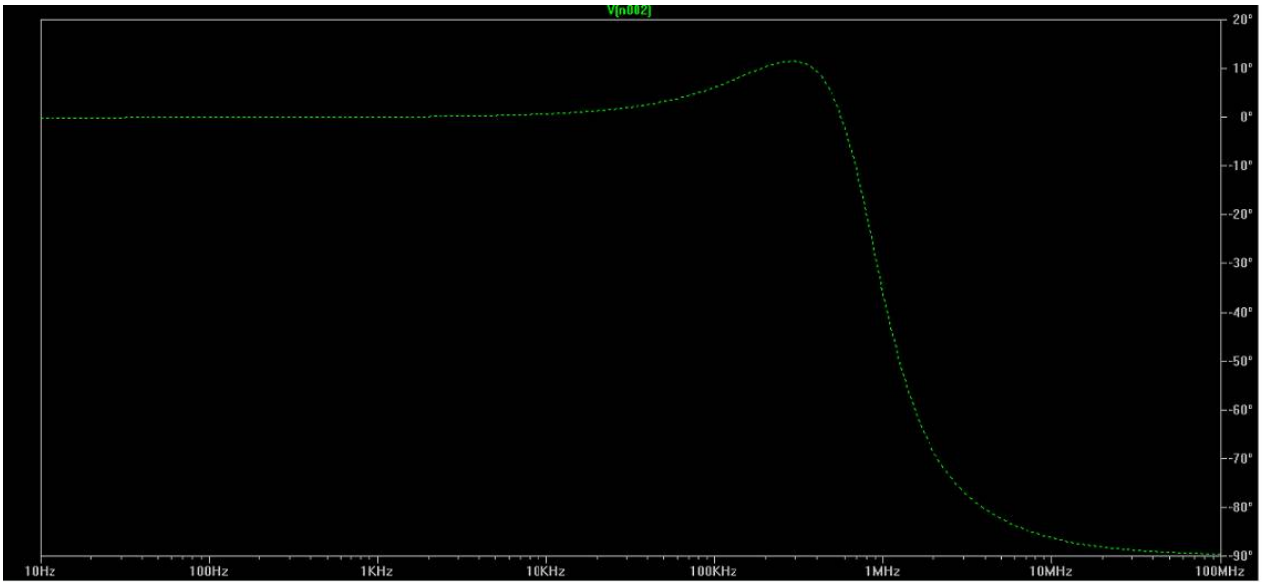

Fig.6. Frequency Analysis of Integrator(op-amp_two stage base)

Simulation Results

- Gain = 71.032 dB;
- cut – off frequency = 1.3 KHz
- Output Swing = 2.48 V ~ - 2.49
- Slew Rate (positive) = 5.12V/us
- Slew Rate (negative) = -5.06V/us

B. Current Mode Integrator

Due to market requirement and the technology constrain, a lot of research has been doing in the area of low voltage(LV) and low power(LP) analog circuit designing. Also, the dramatically growth of submicron technology has been forced the researchers to work at low voltage supply. These LV circuits have to show a reduction of power consumption to maintain a longer battery lifetime. In this area, the obstacles of the voltage-mode signal processing techniques such as the gain-bandwidth product limitation, dynamic range,…etc, are going to be overcome by the current-mode approaches [2,3,4].

The proposed Current conveyor integrator is designed with 0.13µ CMOS technology. An active current mode integrator shown in Fig.7, has been designed for 80dB open loop gain, 100MHz unity gain bandwidth, and 56 deg. phase shift. The strategy in [5] is employed for circuit design. The CMOS inverter is designed with high output impedance (ro) to satisfy an approximately ideal current source, for that both of N- and P- MOST length (L) should be high enough.

The CCII integrator is realized using 1pF feedback capacitor.

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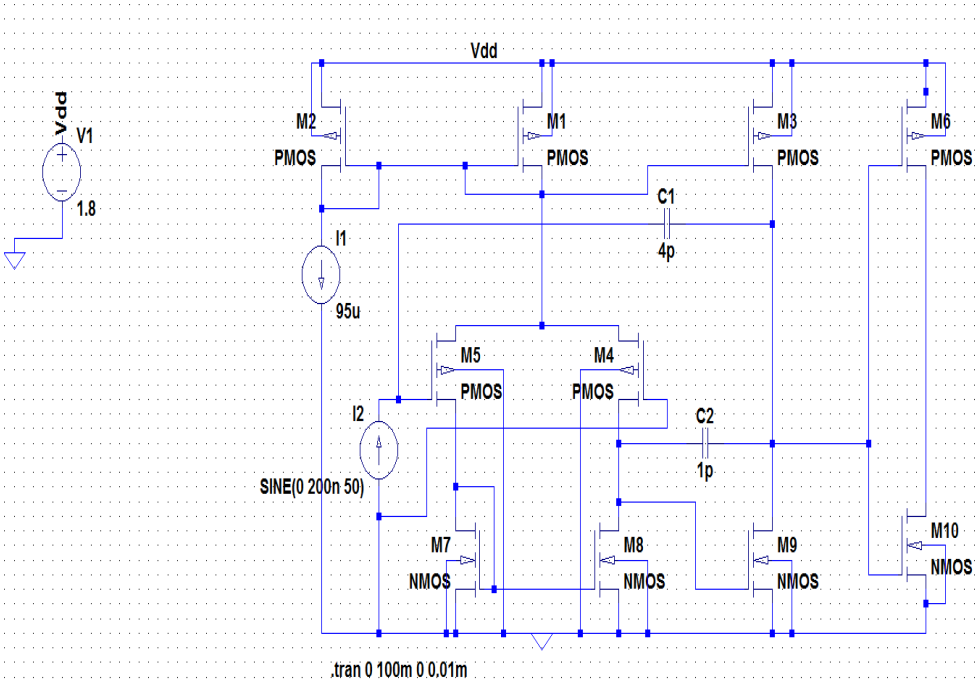

Fig.7.CMOS Based Current Mode Integrator[5]

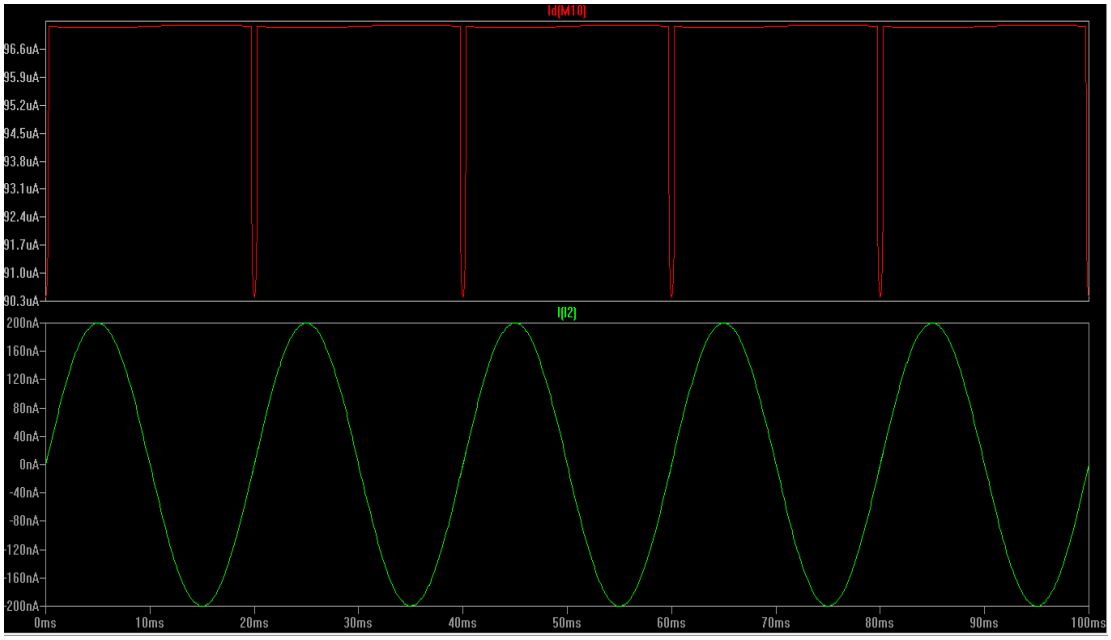

Fig.8. Transient Analysis of Current Mode Integrator

C. Integrator Design with Linear Transconductance Circuit

Linear CMOStransconductors have found widespread use in today's analog microelectronics, and an outstanding number of circuit topologies has been proposed; in order to achieve voltage-to-current conversion, they usually employ

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MOStransistors either operating in saturation or in ohmic (triode) region. In the first case, the MOS Transistor square law is usually exploited in sucha way that linearization is achieved. The second case corresponds to topologies that directly exploit the MOST V-I dependence in triode region for obtaining a linear V-I conversion**,** often leading to transconductors with higher linearity and increased tuning range**.**

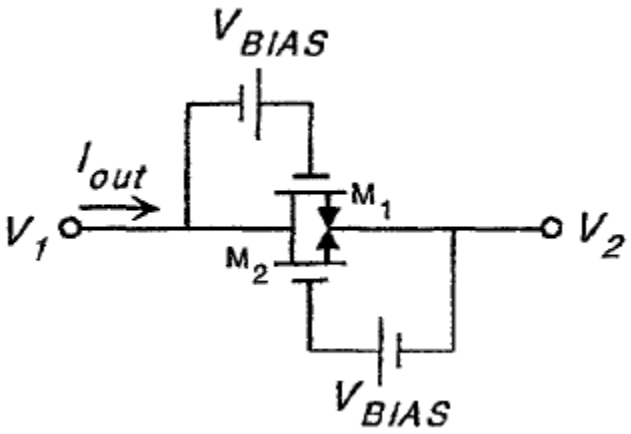

Fig.9. Linearization of MOS Transistor Pair[6]

The basic principle followed for obtaining a linearV-Iconversion is illustrated in below Fig**.** , where both $M_1$and M_2,are identical MOS transistors operating in triode region[7].
Assuming that the simple expression (I) models thedrain current of a triodeMOS,

$$I_d = \beta V_{ds}\left[(V_{gs} - V_{TH}) - \frac{1}{2}V_{ds}\right] \quad \text{with} \quad \beta = \mu C_{ox}\left(\frac{W}{L}\right) \tag{3}$$

The drain currents of M_1 and M_2 are given by

$$I_{d1} = \beta_1(V_1 - V_2)[(V_{BIAS} - V_{TH}) + \frac{1}{2}(V_1 - V_2)] \tag{4}$$

$$I_{d2} = \beta_2(V_1 - V_2)[(V_{BIAS} - V_{TH}) - \frac{1}{2}(V_1 - V_2)] \tag{5}$$

Since $\beta_1 = \beta_2$, a linear dependence on $V_1 - V_2$ is obtained for I_{out}, being the transconductance linearly by the bias voltage V_{BIAS}:

$$I_{out} = I_{d1} + I_{d2} = 2\,\beta_{1,2}(V_{BIAS} - V_{TH}) - (V_1 - V_2) \tag{6}$$

In order to avoid distortion ,M_1 and M_2 should be kept in triode region , and therefore

$$|V_1 - V_2| < V_{BIAS} - V_{TH} \tag{7}$$

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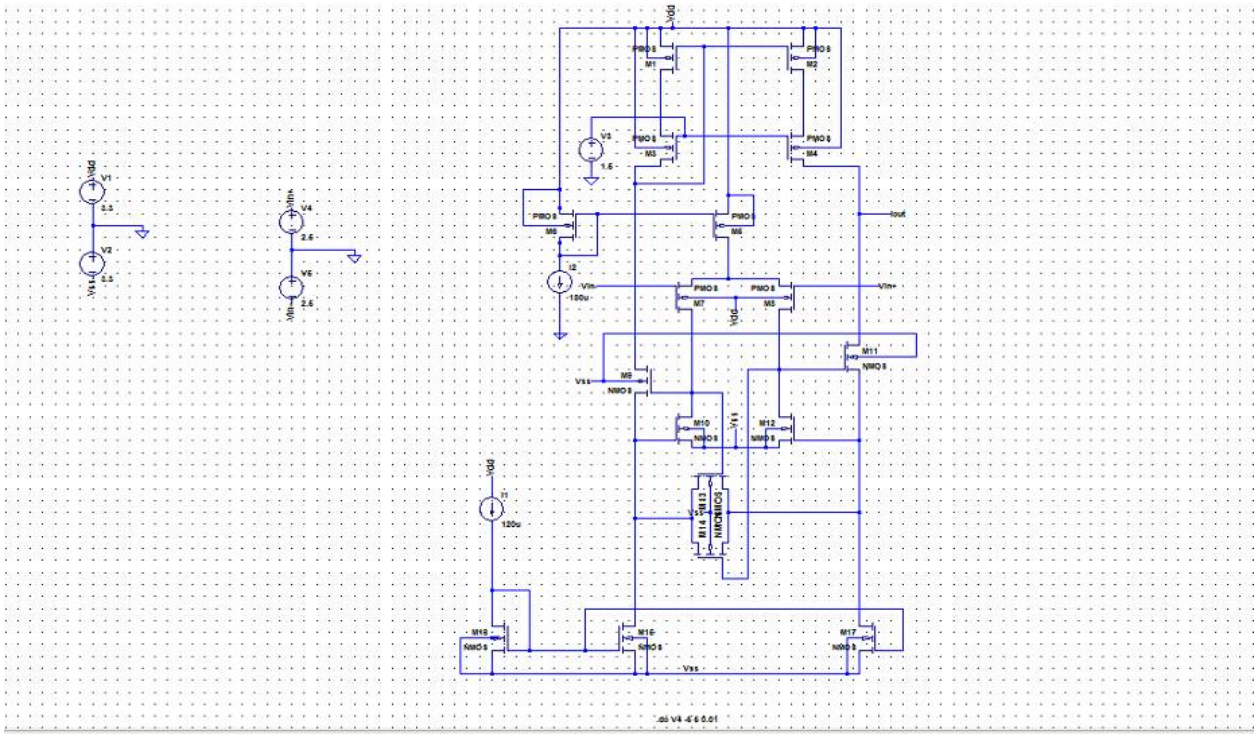

Fig.10. CMOS Integrator(Transconductance based)[6]

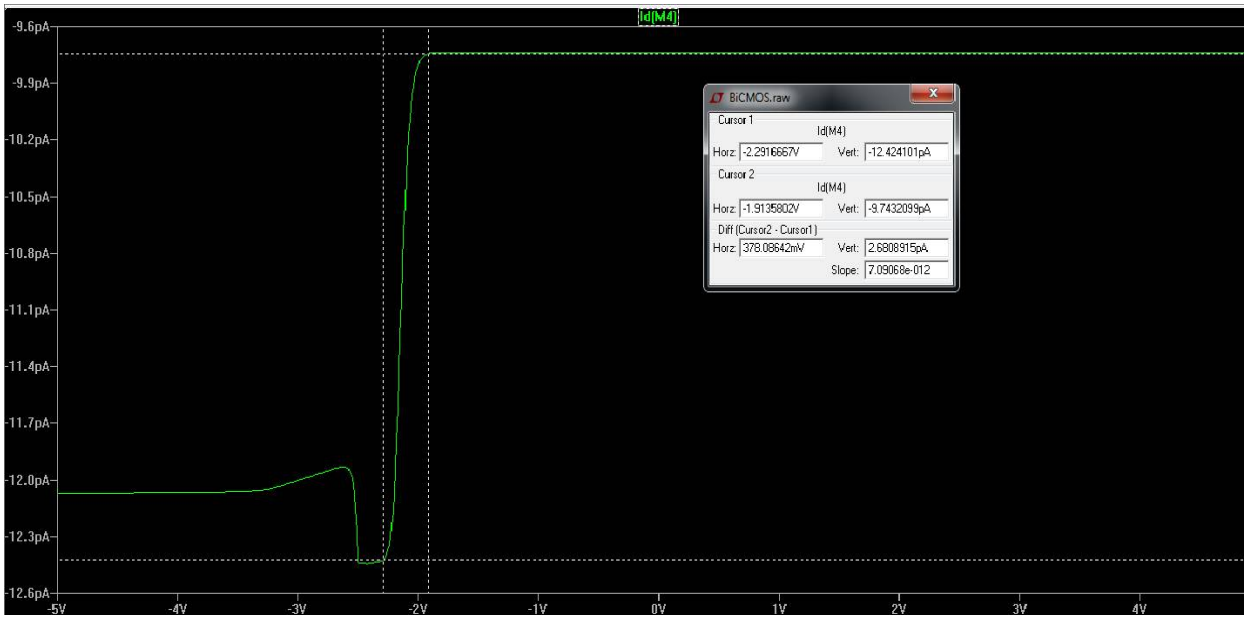

Fig.11. V-I Characteristics Of CMOS Integrator(Transconductance based)

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TABLE 2
COMPARISON OF VARIOUS DESIGN METHODS OF CMOS BASED INTEGRATOR

	Op-amp Based Integrator	**Current Mode Integrator**	**Linear Transconductance circuit based Integrator**
V_{DD}[V]	2.5	1.8	1.8
Technology[nm]	180	130	130
V_{TH}[V]	0.4	0.3	0.3
Power[mW]	1.98	1.1	2.3
f_{-3dB}[KHz]	1.3	1.4	1
Noise[μV_{rms}]	62.9	140.2	70.2

III. CONCLUSION

In this work We have analysedvarious methods of CMOS Based integrator design. Based on application, requirements and design constraints we can follow any of the above methods. i.e. differential op-amp based integrator design is of our choice when we have large gain, sharp cut-off frequency based low pass filter application. In low voltage and low power application our choice will be Current mode Integrator. While if we require linear V-I Characteristics with better bandwidth and noise performance then linear transconductance based integrator approach is useful, however it has low tuning range.

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